

**IN THE CLAIMS**

1. (Canceled)

2. (Canceled)

3. (Canceled)

4. (Canceled)

5. (Previously presented) A system to align digital image data, comprising:  
a plurality of serial data channels, each channel transmitting corresponding serial data,  
the serial data on one serial channel having skew relative to the serial data on other serial  
channels;

a serial to parallel converter to convert the serial data on each of the plurality of serial  
data channels into parallel data on corresponding parallel data channels responsive to a serial  
reference clock; and

an alignment circuit adapted to align the parallel data such that no skew is present  
between the parallel data on one parallel channel and the parallel data on other parallel  
channels responsive to a pixel clock;

wherein the serial to parallel converter generates a pixel clock for each parallel data  
channel and a parallel reference clock;

wherein the alignment circuit comprises:

a queue circuit to store the parallel data on each of the parallel data channels  
responsive to the corresponding pixel clock; and

an alignment detection circuit to detect alignment of the parallel data stored in the  
queue circuit responsive to the parallel reference clock; and

wherein the queue circuit for each of the parallel data channels comprises:

a plurality of FIFO latches, each FIFO latch to store parallel data responsive to the  
corresponding pixel clock;

a compare circuit to generate a match bit for each word of parallel data by monitoring  
the parallel data for a code;

a register circuit to generate a leading edge signal responsive to the corresponding  
pixel clock;

a counter circuit to generate a write pointer responsive to the corresponding pixel clock;

a latch circuit to generate a leading edge pointer by latching the write pointer responsive to the leading edge signal and the corresponding pixel clock; and

a multiplexer circuit to receive parallel data stored in the plurality of FIFO latches and output aligned parallel data to a corresponding parallel data channel responsive to a corresponding read pointer.

6. (Previously presented) The system of claim 5 wherein each FIFO latch stores a word of parallel data responsive to an enable signal; and

wherein the counter circuit generates the enable signal responsive to the corresponding pixel clock.

7. (Previously presented) The system of claim 6 wherein the counter circuit generates the enable signal further responsive to a reset signal.

8. (Original) The system of claim 5 wherein the code is a blanking code.

9. (Previously presented) The system of claim 5 wherein the register circuit generates the leading edge signal by comparing a match bit for a presently stored word of parallel data with a match bit for a previously stored word of parallel data.

10. (Previously presented) The system of claim 5 wherein the alignment detection circuit comprises:

an alignment detection block for each of the parallel data channels, each block to generate the corresponding read pointer responsive to the parallel reference clock; and

a synchronization circuit to receive a leading edge detect signal from each of the alignment detection blocks for each of the parallel data channels and generate a reload read pointer responsive to the parallel reference clock.

11. (Previously presented) The system of claim 10 wherein each alignment detection block comprises:

a shift circuit to receive the corresponding leading edge pointer and generate the corresponding read pointer responsive to the reload read pointer;

a latch to receive the leading edge signal and generate a leading edge detect signal for the corresponding parallel data channel responsive to the reload read pointer.

12. (Previously presented) The system of claim 11 wherein the shift circuit comprises:

a first multiplexer to select between the corresponding leading edge pointer and corresponding read pointer responsive to the reload read pointer;

a shift register to generate a shifted signal by shifting a first multiplexer output signal; and

a second multiplexer to select between the first multiplexer output signal and the shifted output signal responsive to the reload read pointer.

13. (Currently amended) The system of claim 4 5 further comprising a decoder adapted to receive the aligned parallel data on corresponding parallel channels from the alignment circuit, the decoder meeting the digital visual interface specification version 1.0.

14. (Canceled)

15. (Canceled)

16. (Currently amended) The An alignment circuit of claim 15 receiving input parallel data on a plurality of input parallel data channels and generating output parallel data transmissible on a plurality of output parallel data channels, the input parallel data on one input parallel data channel having skew relative to the input parallel data on other input parallel data channels, comprising:

an alignment detection circuit to generate a plurality of read pointers corresponding to the plurality of input parallel data channels responsive to a parallel reference clock signal; and

a plurality of FIFO circuits corresponding to the plurality of input parallel data channels to generate the output parallel data responsive to the plurality of read pointers;

wherein the output data on one output channel has no skew relative to the output data on other output channels;

wherein the alignment detection circuit comprises an alignment detection block for each input data channel, each alignment detection block to generate a read pointer for each input data channel responsive to the parallel reference clock;

wherein each alignment detection block comprises:

a read pointer generating circuit to receive a corresponding leading edge pointer and generate the corresponding read pointer responsive to a reload read pointer signal; and

a latch to receive a leading edge signal and generate a leading edge detect signal for the corresponding input data channel responsive to the reload read pointer signal.

17. (Currently amended) ~~An The alignment circuit of claim 16 receiving input data on a plurality of input data channels and generating output data transmissible on a plurality of output data channels, the input data on one input data channel having skew relative to the input data on other input data channels, comprising:~~

~~an alignment detection circuit to generate a plurality of read pointers corresponding to the plurality of input data channels responsive to a reference clock signal; and~~

~~a plurality of FIFO circuits corresponding to the plurality of input data channels to generate the output data responsive to the plurality of read pointers;~~

~~wherein the output data on one output channel has no skew relative to the output data on other output channels;~~

~~wherein the alignment detection circuit comprises an alignment detection block for each input data channel, each block to generate a read pointer for each input data channel responsive to the parallel reference clock;~~

wherein the read pointer generating circuit comprises:

a first multiplexer to multiplex between the corresponding leading edge pointer and corresponding read pointer responsive to the reload read pointer;

a shift circuit to generate a shifted signal by shifting a first multiplexer output signal; and

a second multiplexer to multiplex between the first multiplexer output signal and the shifted output signal responsive to the reload read pointer.

18. (Previously presented) The alignment circuit of claim 16 wherein the alignment detection circuit further comprises a feedback circuit to generate the reload read pointer signal responsive to the parallel reference clock.

19. (Previously presented) The alignment circuit of claim 18 wherein the feedback circuit comprises:

a logic gate to generate a logic gate signal by logically manipulating leading edge detect signals from each input data channel;

a plurality of serially connected registers to generate the reload read pointer signal by registering the logic gate signal responsive to the parallel reference clock.

20. (Currently amended) ~~The~~ An alignment circuit of claim 14 receiving input parallel data on a plurality of input parallel data channels and generating output parallel data transmissible on a plurality of output parallel data channels, the input parallel data on one input parallel data channel having skew relative to the input parallel data on other input parallel data channels, comprising:

an alignment detection circuit to generate a plurality of read pointers corresponding to the plurality of input parallel data channels responsive to a parallel reference clock signal;  
and

a plurality of FIFO circuits corresponding to the plurality of input parallel data channels to generate the output parallel data responsive to the plurality of read pointers;

wherein the output data on one output channel has no skew relative to the output data on other output channels;

wherein each FIFO circuit comprises:

a plurality of FIFO latches, each FIFO latch to store a word of input data responsive to a corresponding pixel clock;

a compare circuit to generate a match bit for each word of input data by monitoring the input data for a code;

a register circuit to generate a leading edge signal responsive to the corresponding pixel clock;

a counter circuit to generate a write pointer responsive to the corresponding pixel clock;

a latch circuit to generate a leading edge pointer by latching the write pointer responsive to the leading edge signal and the corresponding pixel clock; and

a multiplexer circuit to receive input data stored in the plurality of FIFO latches and output aligned input data to a corresponding input data channel responsive to a corresponding read pointer.

21. (Original) The alignment circuit of claim 20 wherein the code is a DVI blanking code.

22. (Previously presented) The alignment circuit of claim 20 wherein the counter circuit generates an enable signal responsive to the corresponding pixel clock and a reset signal and wherein each FIFO latch is enabled by the enable signal.

23. (Previously presented) The alignment circuit of claim 20 wherein the logic circuit generates the leading edge signal by logically manipulating the match bit of a presently stored data word with a match bit of a previously stored data word responsive to corresponding pixel clock.

24. (Canceled)

25. (Canceled)

26. (Currently amended) The method of claim ~~25~~ 29 wherein receiving the data comprises:

receiving serial data on a plurality of serial channels;  
converting the serial data to parallel data; and  
providing the parallel data to a plurality of parallel channels.

27. (Currently amended) The method of claim ~~25~~ 29 wherein storing the data in a plurality of queues includes for each channel storing a word of data in a plurality of FIFO latches responsive to a corresponding pixel clock.

28. (Canceled)

29. (Currently amended) The A method of claim ~~28~~ for aligning parallel image data, comprising:

receiving the data on a plurality of channels, the data on one channel having skew relative to the data on another channel;

storing the data in a plurality of queues;

detecting a valid data transition by checking the data for a predetermined code;  
setting a read pointer for each channel responsive to the valid data transition; and  
aligning the data by reading the plurality of queues once the read pointers for each of  
the channels point to a valid data transition;  
wherein detecting a valid data transition comprises scanning each word of data for the  
code; and

wherein detecting a valid data transition comprises:  
storing the code for a previous word of data;  
storing the code for a present word of data; and  
comparing the code for the previous with the code for the present word of  
data.

30. (Original) The method of claim 29 wherein detecting a valid data transition includes generating a leading edge signal as a result of comparing the code.

31. (Original) The method of claim 30 wherein detecting a valid data transition includes:  
generating a write pointer responsive to the pixel clock; and  
generating a leading edge pointer by latching the write pointer responsive to the leading edge signal and the pixel clock.

32. (Original) The method of claim 31 wherein setting the read pointer includes:  
generating a reload read pointer by logically manipulating the leading edge signal from each data channel; and  
latching the leading edge pointer responsive to the reload read pointer.

33. (Original) The method of claim 32 wherein aligning the data by reading the plurality of queues includes:  
multiplexing data from the plurality of FIFO latches to a corresponding data channel responsive to the read pointer, wherein multiplexed data provided to one data channel is aligned relative to other multiplexed data provided to other data channels.